

REMARKS/ARGUMENTS

Claims 1-21 stand rejected under 35 U.S.C. §102 over U.S. Patent 4,720,812 (Kao). Claims 3 through 7, 10-11, 14-17, and 20-21 stand rejected under 35 U.S.C. §103(a) as unpatentable over Kao in further view of U.S. Patent 5,802,550 (Fullam).

Integrated Processor System

The present invention as set forth in independent claims 1 and 12 provides an "integrated processor system", that is, a processor system having components on the same integrated circuit as described at paragraph [0005] of the present specification. Per claims 1 and 12, the integrated processor system must include (1) a processing unit; (2) a non-volatile boot memory; and (3) an internal system storage structure selected from the group consisting of: caches, buffers, and registers.

Kao is not an integrated processor system as required by claims 1 and 12, being instead, an architecture composed of separate integrated circuits for microprocessor 50, the PROM 58 (the boot memory) and the latch (buffer 64). This is evident from the specification, and in particular, the recitation of the microprocessor (TI 320) described at col. 5, line 29 which is a single integrated circuit microprocessor without a non-volatile boot memory manufactured by Texas Instruments.

The significance of the limitation of an "integrated processor system" is described in the Background of the Invention section of the present application. In such integrated processor systems, random access memory (RAM) must normally be external to the integrated processor system for reasons of cost, size, and flexibility. See paragraph [0006]. When the integrated processor system is "booted" from its internal boot memory, it normally must communicate with this external memory, and this requires the bootstrap program to know in advance the type of external memory being used. See paragraph [0008]. Presupposing in the bootstrap program, a single type of memory, severely limits the ability to use different memory types with the integrated processor system.

The present invention allows the integrated processor system to perform some of the boot process without communicating with external memory using internal registers as if they were external memory so that the boot process itself may determine the type of external memory, and therefore successfully communicate with a variety of different memory types. See generally paragraph [0010].

Kao does not execute a portion of the bootstrap program using an internal system storage without access to external memory. The bootstrap program itself is in external memory 58 as shown in Fig. 3 and external memory 56 is expressly used for its execution. See generally col. 9, lines 21-42 describing execution of the boot strap program which requires the boot strap copying data from the PROM into the main memory 56.

Importantly, there is no teaching or motivation in Kao for having the bootstrap program be able to execute without access to the main memory because the system of Kao contemplates that the type of external memory will be fixed and known by the bootstrap program.

Thus, with respect to claims 1 and 12, Kao also fails to teach the processing unit executing a portion of the boot strap program using an internal system storage for temporary storage without access to external memory.

Fullam does not remedy these deficiencies. Although Fullam (at Fig. 3) teaches an integrated processor 50 having some internal storage structure 54, the boot memory is an external device 58. See col. 7 lines 27-31. Thus like Kao, Fullam fails to teach an integrated processor system having a process unit and a non-volatile boot memory.

More importantly, Fullam teaches away from the idea of allowing the bootstrap program to partially execute without access to external memory by assuming that the integrated processing system can access external memory during the boot process by using a "default" mode. See col. 7 lines 30-36. This eliminates the need for using internal memory structures for booting as claimed by the present invention. Thus Fullam teaches away from the idea that an integrated processor system having an internal boot memory can execute without access to external

memory in order to determine the type of external memory to which it must interface.

Because neither Kao nor Fullam alone or in combination teach the limitations of independent claims 1 and 12, the remaining claims are also allowable over these references and Applicants respectfully request rejection of these claims be withdrawn.

In view of the remarks set forth herein, the application is believed to be in condition for allowance and notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the examiner is requested to contact the undersigned attorney with any questions, comments or suggestions relating to the referenced patent application.

It is believed that no fee is due as a result of this response. However, the Commissioner is authorized to charge any fees under 37 CFR § 1.17 that may be due on this application to Deposit Account 17-0055. The Commissioner is also authorized to treat this amendment and any future reply in this matter requiring a petition for an extension of time as incorporating a petition for extension of time for the appropriate length of time as provided by 37 CFR § 136(a)(3).

Respectfully submitted,

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